XINERTEL
信而泰

DarSen210

800G Optical Network Tester

DarSen210 Chassis

With the rapid advancement of artificial intelligence (AI), data centers are experiencing growing demand for ultra-high-speed networks. As the core component of these networks, 800GE optical modules play a pivotal role in ensuring stable data center operations. However, their production process faces complex technical challenges and high failure risks. To guarantee long-term operational stability and reliability, extended-duration reliability testing has become an indispensable phase in manufacturing, simulating real-world network conditions to expose potential material defects, process flaws, or design shortcomings—effectively eliminating early failure risks before product deployment.

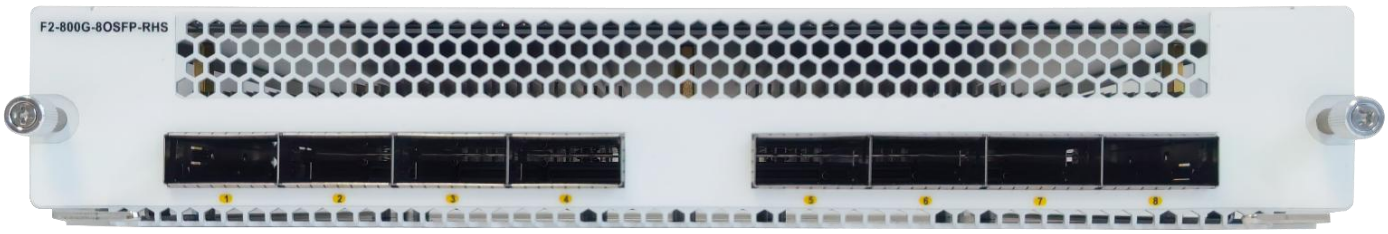
To efficiently execute prolonged reliability testing for 800GE optical modules during production, XINERTEL introduces the DarSen210 platform. This solution supports: BER testing, FEC analysis, PHY-layer equalization tuning, Real-time monitoring etc. Helps manufacturers enhance product quality, reduce failure rates, and accelerate the development of high-speed networks for the AI era.

Key Features

- Chassis provides 2 slots, dimensions: 442 x 113.2 x 500mm (W x H x D)
- Port types: OSFP/OSFP-RHS/ QSFP-DD , supports 1.6T iteration
- Supports multi-chassis cascading for scalable testing
- Clock synchronization capability
- Multiple management IP modification methods
- Browser/Server (B/S) architecture software, ready to use out of the box
- Provides WebAPI for secondary development, compatible with any OS

F2-800G Series Test Modules

- The 800G Series Board is Xinertel's next-generation 800GE Ethernet test module with a globally leading architecture. The F2-800G series supports flexible interface configurations (1×800G/2×400G/4×200G/8×100G) and delivers Ethernet L1 testing capabilities. It addresses critical requirements for long-duration reliability testing (e.g., bit error rate analysis) and performance validation of 800G/400G/200G/100G high-speed optical transceivers.



Key Features

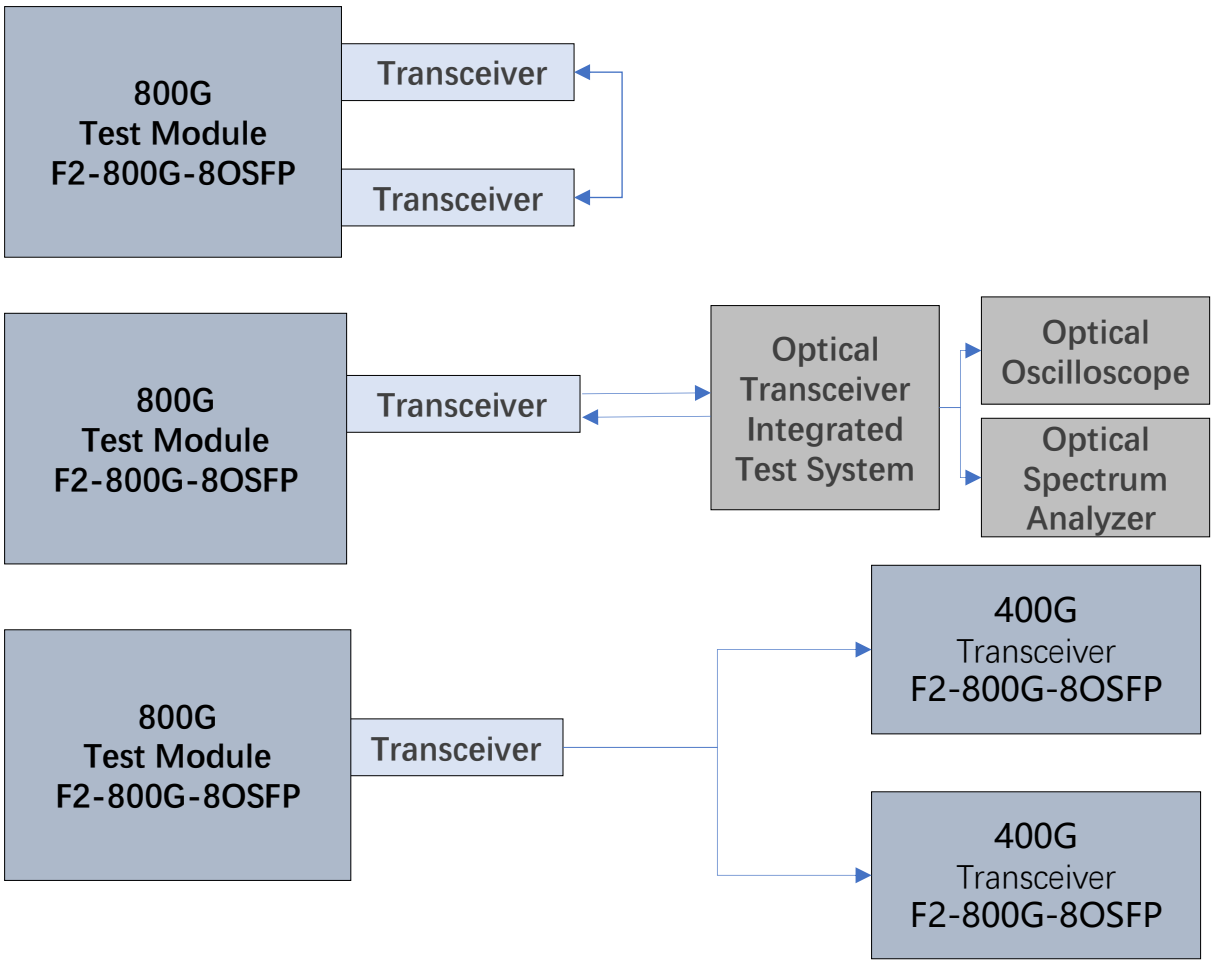
- **Rich Interface Types**
  - 8 ports per card: OSFP/OSFP-RHS/QSFP-DD （Optional）
  - Single-port max bandwidth: 800G (8*112G),
  - Support 1*800G、2*400G、4*200G、8*100G
- **Comprehensive Layer 1 Testing**
  - Bit error rate (BER) testing for rapid fault localization.
  - FEC analysis to evaluate error correction and optimize performance.
  - PHY equalization tuning to enhance signal quality.
  - PPM clock offset testing to ensure synchronization.
  - Voltage Margin Testing to Validate optical module stability
  - Real-Time monitor(temperature, optical power, power consumption etc.) monitoring for Transceiver stability.
  - I2C Interface Stress Testing to emulate I2C bus anomalies.
  - Real-Time Optical Monitoring: Track Tx/Rx optical power, bias current, and module temperature etc.
  - Comprehensive Test Logging: BER statistics, FEC statistics, temperature, voltage etc. and export detailed reports for failure root cause analysis.

Specifications

Module Name	**F2-800G-8OSFP Test Module** **F2-800G-8OSFP-RHS Test Module** **F2-800G-8QSFP Test Module**
Service Characteristics	
Port Speed	Up to 800GE per port, up to 12 x 800GE-Ports per Chassis Support 1*800G、2*400G、4*200G、8*100G
Port density	Supports 8 ports: : OSFP/OSFP-RHS/QSFP (Optional)
Lane Speed	PAM4: 112G/106G/56G/53G NRZ : 28~25G
PRBS	PRBS9, PRBS13, PRBS15, PRBS31, etc.
BER Statistic Item	Supports per-lane statistics for: Error count/Bit Error Rate (BER) Pre-FEC error count/BER, Post-FEC error count/BER; Records timestamps (in seconds) for min/max extreme values
FEC Perform Analyze	Supports per-lane statistics for: Symbol Error distribution, FEC Margin; Records timestamp (in seconds) of first Symbol Error occurrence
DDM Monitor	Supports temperature, power consumption monitoring, Records timestamps (in seconds) for min/max extreme values
I2CStress Test	Supports optical transceiver pin control, register read/write, and I2C stress test.
Voltage Margin	Supports Power Supply Voltage Margin Test(±600mv)
Frequency Offset (PPM)	±500PPM, Accuracy: 1PPM
PHY Equalization Tuning	Supports per-lane Tx Taps customization Enables automatic Tx Taps scanning & optimization
Test Report	Comprehensive Test Logging : error events, FEC statistics etc. and export detailed reports for failure root cause analysis.
Electrical Characteristics	
Dimensions	280mm x 45.32mm x 369mm (W x H x D)
Power	≤400W

Typical Application Scenarios

■ Optical Transceiver Test Scenarios



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